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10/626,756	07/24/2003	Kevin Traynor	032674-200	1739

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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,756	TRAYNOR ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Allowable subject matter is withdrawn in view of further consideration of the prior arts on record during the pre-appeal conference on 4/27/2006. A new set of Rejection follows.

Claim Objections

2. Claims 6, 12, and 18 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 6, 12, and 18 claim at least one interrupt source and at least one interrupt input. Claims 6, 12, and 18 fail to further limit the subject matter of a parent claim because the parent claims claim a plurality of interrupt sources and a plurality of interrupt inputs.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Suh (U.S. Patent No. 6,742,065).

Referring to claims 1 and 7: Suh discloses an interrupt controller and a method of accessing interrupts. Suh discloses mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs (figure 3, mapping is0..is25 to INT1 and INT2). Suh discloses a mask register (figure 1, structure 10, column 3, lines 39-45) to selectively enable the interrupt request. Hence, claim is anticipated by Suh.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-4, 6-10, 12-17, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Giles et al. (U.S. Patent No. 6,070,218) and Suh.

Referring to claim 1: Giles discloses mapping each of the plurality of interrupt sources to interrupt input (figures 4-5, mapping SOFTINT0..1 and INTPIN0..INTPIN5 to INTERRUPT PROCESSOR); and selectively enabling interrupt requests from each of the plurality of interrupt sources to interrupt input (figures 4-5, SOFTINT0EN..INTPIN5EN to selectively enable each interrupt request). Giles does not explicitly disclose a plurality of interrupt inputs. Suh discloses selectively mapping each of the interrupt requests (figure 3, is0..is25) to each of a plurality of interrupt inputs (figure 3, INT1 and INT2). Suh teaches one to increase the system performance by increasing the capacity and resources for processing the interrupts. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Suh's teaching onto Giles because Suh teaches one to increase the system performance by increasing the capacity and resources for processing the interrupts.

Referring to claim 2: Giles discloses determining a value of control bits (figures 4-5, SOFTINT0EN..INTPIN5EN) respectively associated with each mapped interrupt source/interrupt input combination; and selectively enabling interrupt requests between the mapped interrupt source/interrupt input combinations according to the respective control bit values (figures 4-5, AND gates 504 and 506).

Referring to claim 3: Giles discloses determining a value of a control bit associated with a mapped interrupt source/interrupt input combination (figures 4-5, each AND gate 504 or 506

receives the control bit/enable bit) and selectively enabling interrupt requests between the mapped interrupt source/interrupt input combination according to the associated control bit value (figures 4-5, each AND gate 504 or 506 selectively enable the interrupt request according to the control/enable bit), repeating steps a and b until control bit values for all mapped interrupt source/interrupt input combinations are determined and enabled/disabled accordingly (figures 4-5, one AND gate for each interrupt request).

Referring to claim 4: Suh discloses setting the control bit values according to user preferences (column 3, lines 39-46).

Referring to claim 6: Giles discloses defining the control bit values according to system requirements (figures 4-5, one control bit and AND gate for each interrupt request). Giles further discloses processor (figure 1, CPU CORE), at least one interrupt source (figures 4-5, SOFTINT0), and at least one interrupt input (figures 4-5, TO INTERRUPT PROCESSO).

Referring to claim 7: Giles discloses mapping each of the plurality of interrupt sources to interrupt input (figures 4-5, mapping SOFTINT0..1 and INTPIN0..INTPIN5 to INTERRUPT PROCESSOR); and selectively enabling interrupt requests from each of the plurality of interrupt sources to interrupt input (figures 4-5, SOFTINT0EN..INTPIN5EN to selectively enable each interrupt request). Giles does not explicitly disclose a plurality of interrupt inputs. Suh discloses selectively mapping each of the interrupt requests (figure 3, is0..is25) to each of a plurality of interrupt inputs (figure 3, INT1 and INT2). Suh teaches one to increase the system performance by increasing the capacity and resources for processing the interrupts. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the

invention to adapt Suh's teaching onto Giles because Suh teaches one to increase the system performance by increasing the capacity and resources for processing the interrupts.

Referring to claim 8: Giles discloses determining a value of control bits (figures 4-5, SOFTINT0EN..INTPIN5EN) respectively associated with each mapped interrupt source/interrupt input combination; and selectively enabling interrupt requests between the mapped interrupt source/interrupt input combinations according to the respective control bit values (figures 4-5, AND gates 504 and 506).

Referring to claim 9: Giles discloses determining a value of a control bit associated with a mapped interrupt source/interrupt input combination (figures 4-5, each AND gate 504 or 506 receives the control bit/enable bit) and selectively enabling interrupt requests between the mapped interrupt source/interrupt input combination according to the associated control bit value (figures 4-5, each AND gate 504 or 506 selectively enable the interrupt request according to the control/enable bit), repeating steps a and b until control bit values for all mapped interrupt source/interrupt input combinations are determined and enabled/disabled accordingly (figures 4-5, one AND gate for each interrupt request).

Referring to claim 10: Suh discloses setting the control bit values according to user preferences (column 3, lines 39-46).

Referring to claim 12: Giles discloses defining the control bit values according to system requirements (figures 4-5, one control bit and AND gate for each interrupt request). Giles further discloses processor (figure 1, CPU CORE), at least one interrupt source (figures 4-5, SOFTINT0), and at least one interrupt input (figures 4-5, TO INTERRUPT PROCESSO).

Referring to claim 13: Giles discloses that each mapped interrupt source/interrupt input combination has a logical AND for ANDing each interrupt source with a respective control bit value (figures 4-5).

Referring to claim 14: Giles discloses, for each interrupt input, a plurality of logical ANDs (figures 4-5, AND gates 504 and 506), each corresponding to an interrupt source, the corresponding interrupt source providing an interrupt request signal to the corresponding logical AND to interrupt the processor; a plurality of control bits (figures 4-5, SOFTINT0EN..INTPIN5EN) each corresponding to an interrupt source and each respectively providing a control bit value to the corresponding logical AND, wherein, based on the control bit value, a corresponding interrupt request signal is provided at an output of the corresponding logical AND; a logical OR (figures 4-5, OR gates 408 and 508) arranged to indicate, to the interrupt input, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical ANDs. Giles does not explicitly disclose a plurality of interrupt inputs. Suh discloses selectively mapping each of the interrupt requests (figure 3, is0..is25) to each of a plurality of interrupt inputs (figure 3, INT1 and INT2). Suh teaches one to increase the system performance by increasing the capacity and resources for processing the interrupts. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Suh's teaching onto Giles because Suh teaches one to increase the system performance by increasing the capacity and resources for processing the interrupts.

Referring to claim 15: Suh discloses a register (figure 3, structure 10) for storing the control bit values.

Referring to claim 16: Suh discloses setting the control bit values according to user preferences (column 3, lines 39-46).

Referring to claim 18: Giles discloses defining the control bit values according to system requirements (figures 4-5, one control bit and AND gate for each interrupt request). Giles further discloses processor (figure 1, CPU CORE), at least one interrupt source (figures 4-5, SOFTINT0), and at least one interrupt input (figures 4-5, TO INTERRUPT PROCESSO).

Referring to claim 19: Giles that the processor is part of a microcontroller unit (figure 1).

Referring to claim 20: Giles discloses that the number of interrupt sources is greater than the number of interrupt inputs (figure 4-5).

9. Claims 5, 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Giles, Suh, and Monahan et al. (U.S. Patent No. 4,001,783).

Referring to claims 5, 11, and 17: Giles and Suh's disclosures are stated above; neither of them explicitly discloses setting the control bit values dynamically according to user preference. Monahan discloses a programmable interface application to configure interrupt processing related information while system is in operation (column 3, lines 10-14). Monahan teaches one to further adjust the system performance by customize priority for each interrupt request source. Hence, it would have been obvious to one having ordinary skill in the computer art to adopt Monahan's teaching onto Giles and Suh because Monahan teaches one to implement a system with flexibility allowing user to further adjust the system performance by dynamically customize priority for each interrupt request source.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests

to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
May 9, 2006

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